Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1 to 11. (Canceled).

12. (Previously Presented) A system for reconfiguring a programmable unit, the programmable unit including a plurality of reconfigurable function cells in a multidimensional arrangement, comprising:

a primary logic unit in communication with at least one of the plurality of reconfigurable function cells, the primary logic unit configured to detect an event and to detect a state of the at least one of the plurality of reconfigurable function cells;

a first memory configured to store a first configuration data associated with a selected one of the plurality of reconfigurable function cells;

a jump table coupled to the primary logic unit having a plurality of entries, at least one of the plurality of entries configured to store a memory address of the first configuration data; and

a FIFO memory shared by the plurality of reconfigurable function cells and coupled to the primary logic unit configured to store a plurality of configuration data associated with the plurality of reconfigurable function cells, the plurality of configuration data including the first configuration data.

13. (Previously Presented) The system according to claim 12, wherein, when the primary logic unit detects the event, the primary logic unit reads the FIFO memory to determine whether a configuration data from the plurality of configuration data is stored in the FIFO memory.

14. (Previously Presented) The system according to claim 13, wherein, when the primary logic unit determines that no configuration data is stored in the FIFO memory, the primary logic unit retrieves the memory address, retrieves the first configuration data from the first memory based on the memory address, reconfigures the selected one of the plurality of reconfigurable function cells based on the configuration data if the selected one of the plurality of reconfigurable function cells is in a reconfigurable state, and stores the first reconfiguration data in the FIFO memory if the selected one of the plurality of reconfigurable function cells is not in a reconfigurable state.

15. (Previously Presented) The system according to claim 13, wherein, when the primary logic unit determines that some configuration data from the plurality of configuration

data is stored in the FIFO memory, if the first configuration data is not stored in the FIFO memory, the primary logic unit retrieves the first configuration data from the first memory based on the memory address, and stores the first configuration data in the FIFO memory.

Claim 16. (Canceled).

17. (Previously Presented) The system according to claim 13, wherein, when the primary logic unit determines that some configuration data from the plurality of configuration data is stored in the FIFO memory, if the first configuration data is stored in the FIFO memory and is not the first entered into the FIFO memory, the primary logic unit does not retrieve the first configuration data.

18. (Previously Presented) A method for reconfiguring a programmable unit, the programmable unit including a plurality of reconfigurable function cells in a multidimensional arrangement, comprising:

detecting an event and a state of at least one of the plurality of reconfigurable function cells;

storing, in a first memory, a first configuration data associated with a selected one of the plurality of reconfigurable function cells;

storing a memory address of the first configuration data; and

storing, in a FIFO memory shared by the plurality of reconfigurable function cells, a plurality of configuration data associated with the plurality of reconfigurable function cells, that includes the first configuration data.

19. (Previously Presented) The method according to claim 18, wherein, when detecting the event, the FIFO memory is read to determine whether a configuration data from the plurality of configuration data is stored in the FIFO memory.

Claim 20. (Canceled).

21. (Previously Presented) The method according to claim 19, wherein, when determining that no configuration data is stored in the FIFO memory, the memory address is retrieved, the first configuration data is retrieved from the first memory based on the memory address, and, if the selected one of the plurality of reconfigurable function cells is not in a reconfigurable state, the first reconfiguration data is stored in the FIFO memory.

22. (Previously Presented) The method according to claim 19, wherein, when determining that some configuration data from the plurality of configuration data is stored in the FIFO memory, if the first configuration data is not stored in the FIFO memory, the first configuration data is retrieved from the first memory based on the memory address, and is stored in the FIFO memory.

23. (Previously Presented) The method according to claim 19, wherein, when the determining that some configuration data from the plurality of configuration data is stored in the FIFO memory, if the first configuration data is the first entered into the FIFO memory, the first configuration data is retrieved from the FIFO memory.

24. (Previously Presented) The method according to claim 19, wherein, when determining that some configuration data from the plurality of configuration data is stored in the FIFO memory, if the first configuration data is stored in the FIFO memory and is not the first entered into the FIFO memory, the first configuration data is not retrieved.

25. (Previously Presented) A system for run-time reconfiguration of a programmable unit, the programmable unit including a plurality of reconfigurable function cells in a multi-dimensional arrangement, comprising:

a primary logic unit in communication with at least one of the plurality of reconfigurable function cells, the primary logic unit configured to detect an event and to detect a state of the at least one of the plurality of reconfigurable function cells;

a first memory configured to store a first configuration data associated with a selected one of the plurality of reconfigurable function cells;

a jump table coupled to the primary logic unit having a plurality of entries, at least one of the plurality of entries configured to store a memory address of the first configuration data, wherein when the primary logic unit detects the event, the primary logic unit calculates the address of the at least one of the plurality of entries in the jump table based on a source of the event, retrieves the memory address, and retrieves the stored first configuration data based on the memory address; and

a FIFO memory shared by the plurality of reconfigurable function cells and coupled to the primary logic unit configured to store a plurality of configuration data associated with the plurality of reconfigurable function cells, the plurality of configuration data including the first configuration data, the first configuration data stored in the FIFO memory if the selected one of the plurality of reconfigurable function cells is not in a reconfiguration state, and the primary logic unit configured to reconfigure the selected one of the plurality of reconfigurable function cells if the selected one of the plurality of reconfigurable function cells is in a reconfigurable state.

26. (Previously Presented) The system according to claim 25, wherein the first memory is configured to store a plurality of configuration data, at least one configuration data from the plurality of configuration data including a complete configuration of the at least one of the plurality of reconfiguration function cells.

27. (Previously Presented) The system according to claim 25, wherein the first memory is configured to store at least one subconfiguration data configured to represent only

a part of a complete configuration of the at least one of the plurality of reconfiguration function cells.

28. (Previously Presented) The system according to claim 25, wherein the primary logic unit contains a start configuration register which points to a start configuration that puts the at least one of the plurality of reconfiguration function cells in a valid state.

29. (Previously Presented) The system according to claim 25, wherein the primary logic unit contains a FIFO start register which points to a start of a memory area to which a configuration data is copied.

30. (Previously Presented) The system according to claim 25, wherein the primary logic unit contains a FIFO end register which points to an end of a memory area to which a configuration data is copied.

31. (Previously Presented) The system according to claim 25, wherein the primary logic unit contains a FIFO free entry register which points to a free entry of a memory area to which a configuration data is copied and which is closest to a start of the memory area.

32. (Previously Presented) The system according to claim 25, wherein the primary logic unit contains a program counter register which points to an entry to be processed within the first memory.

33. (Previously Presented) The system according to claim 25, wherein the primary logic unit contains an address register which points to an address of the cell which has triggered the event.

34. (Previously Presented) The system according to claim 25, wherein the primary logic unit contains a data register containing a configuration data which is transmitted to the at least one of the plurality of reconfiguration function cells in a reconfiguration.

35. (Previously Presented) The system according to claim 25, wherein the primary logic unit contains a dispatch register which contains the address of an entry in the jump table calculated from a cell address.

36. (Currently Amended) A system for reconfiguring a programmable unit, the programmable unit including a plurality of reconfigurable function cells in a multidimensional arrangement, comprising:

a primary logic unit for reconfiguring at least a selected one of the plurality of function cells and in communication with at least one of the plurality of reconfigurable

function cells, the primary logic unit configured to detect an event when in communication with the at least one of the plurality of reconfigurable function cells;

a first memory configured to store a configuration data associated with at least the selected one of the plurality of function cells;

a FIFO memory shared by the plurality of reconfigurable function cells; and

a selection unit for selecting the configuration data from the first memory in response to the detection of the event,

wherein the primary logic unit is configured to check a reconfigurability state of the selected one of the plurality of function cells, reconfigure ~~before reconfiguring~~ the selected one of the plurality of function cells according to the selected configuration data upon a condition that the selected one of the plurality of function cells is in a reconfigurable state, and otherwise store the selected configuration data in the FIFO memory.

37. (Currently Amended) A method for deadlock-free run-time reconfiguration of a programmable unit, the programmable unit including a plurality of reconfigurable function cells in a multidimensional arrangement, comprising:

detecting an event;

selecting at least one of the plurality of reconfigurable function cells in response to the detected event;

reading entries of a FIFO memory shared by the plurality of reconfigurable function cells and that stores configuration data associated with the plurality of reconfigurable function cells;

determining ~~which~~ whether configuration data associated with the selected at least one function cell is stored in the FIFO memory;

in response to a determination that [[a]] the configuration data associated with the selected at least one function cell is not stored in the FIFO memory and upon a condition that the determination is made, retrieving [[the]] configuration data associated with the selected at least one function cell from another configuration memory; and

if a state of the selected at least one function cell is not a reconfiguration state, storing the retrieved configuration data in the FIFO memory.

38. (New) The system according to claim 13, wherein, when the primary logic unit determines that some configuration data from the plurality of configuration data is stored in the FIFO memory, if the first configuration data is the first entered into the FIFO memory, the primary logic unit retrieves the first configuration data from the FIFO memory.

39. (New) The method according to claim 19, wherein, when determining that no configuration data is stored in the FIFO memory, the memory address is retrieved, the first

configuration data is retrieved from the first memory based on the memory address, and, if the selected one of the plurality of reconfigurable function cells is in a reconfigurable state, the selected one of the plurality of reconfigurable function cells is reconfigured based on the configuration data.